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Caven & Aghevli LLC
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402

| EXAMINER |
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| HUSSAIN, TAUQIR |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## DETAILED ACTION

### *Response to Amendment*

1.     This office action is in response to amendment /reconsideration filed on

10/14/2009, the amendment/reconsideration has been considered. Claims 4 and 21

have been cancelled, claim 1 has been amended and claims 34-36 have been newly

added. Therefore, Claims 1, 2, 5, 7-19 and 23-36 are pending for examination, the

rejection cited as stated below.

### *Response to Arguments*

2.     Applicant's arguments filed on 10/14/2009 have been fully considered but they

are not deemed to be persuasive. In the remarks, applicant argued in substance that

(a)     Prior art "Viswanath and Malakapalli" does not teach, "determining

whether to edit the frame prior to providing to the second port", where the VLAN

tag is to be inserted "based on the determination of whether to edit the frame".

As to point (A), Examiner respectfully disagrees and suggest the teaching from

the cited prior art Viswanath as disclosed in Col.2, lines 50-56, The present invention

addresses the above noted needs and drawbacks of current network switches in part by

providing an integrated multiport switch that will determine whether packets received at

designated VLAN ports are tagged packets. If so, the VLAN tag is stripped from the

packet before further processing the incoming data at the media access controller of the

port. Viswanath further disclosed in Col.3, lines 4-14, where VLAN tags are inserted in

untagged or stripped packets that are to be transmitted at a VLAN port, which means

there is already a criteria for determining whether the packet is tagged or untagged

which is same as determining whether to edit the frame as discussed above and Col.7,

lines 42-45, where one or more VLAN destination stations have VLAN tags inserted,

unless the tagging is selectively overridden by the rules checker before transmitting it to

second/output port and further selectively overridden is equivalent to determining

whether to edit the frame or not.).

### *Claim Objections*

3.      Claims 34-36 are objected to because of the following informalities:  Claims 34-

36 recite "wherein one or more **question** are to be segmented......". Examiner will read

the claim as "wherein one or more queues are to be segmented....." for examining

purposes.  Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

4.      The text of those sections of Title 35, U.S. Code not included in this action can

be found in a prior Office action.

5.      <u>Claims 1, 2, 4, 5, 7-19, 21 and 23-33 are rejected under 35 U.S.C. 103(a) as</u>

<u>being unpatentable over Viswanath et al. (Patent Number: 6151322), hereinafter</u>

<u>"Viswanath" in view of</u> Malakapalli et al. (Patent. No.: US 6,467,060 B1), hereinafter

"Malakapalli".

6.      As to claim 1, Viswanath discloses, receiving electronic data from a first port of

the data networking device (Viswanath, Abstract, lines 1-2);

        discarding at least a portion of the electronic data prior to providing the electronic

data to a memory of the networking device wherein the portion of electronic data

deleted comprises a VLAN (virtual local area network) tag; (Abstract, lines 3-10, where

striping the tag means discard the portion of the electronic data and Col.7, lines 10-13,

where VLAN tag is extracted means discarded and only VLAN ID is stored with frame in

a memory);

      providing at least a portion of the electronic data to a second port (Viswanath,

Abstract, lines 16-20, where transmitting port is the second port).

      generating a code and inserting the code into the frame prior to providing to the

memory (Viswanath, Fig.4, Elements-84 and 64, Col.7, lines 21-39, where tagging can

be interpret as coding and modifying means adding or deleting or inserting the

appropriate information into frame and sending it to memory 64).

      Determining  whether to edit the frame prior to providing to the second port,

wherein a value of the VLAN tag to be inserted into the frame prior to providing to the

second port based on the determination of whether to edit the frame (Viswanath, Col.6,

lines 3-22, where VLAN tag is inserted before sending it to transmit to the second or

output port and further Col.2, lines 50-56, The present invention addresses the above

noted needs and drawbacks of current network switches in part by providing an

integrated multiport switch that will determine whether packets received at designated

VLAN ports are tagged packets. If so, the VLAN tag is stripped from the packet before

further processing the incoming data at the media access controller of the port

Viswanath further discloses in Col.3, lines 4-14, where VLAN tags are inserted in

untagged or stripped packets that are to be transmitted at a VLAN port, which means

there is already a criteria for determining whether the packet is tagged or untagged

which is same as determining whether to edit the frame as discussed above and Col.7,

lines 42-45, where one or more VLAN destination stations have VLAN tags inserted,

unless the tagging is selectively overridden by the rules checker before transmitting it to

second/output port and further selectively overridden is equivalent to determining

whether to edit the frame or not.).

Viswanath however is silent on disclosing generating CRC and inserting CRC

into a frame or checking the CRC prior to providing to the second port.

Malakapalli however discloses, generating CRC and inserting CRC into a frame

(Malakapalli, Col.17, lines 32-49, where CRC generator generates the first CRC and

seed it in logical block addresses and Col.17, lines 50-65, Comparator compares the

CRC before sending it to output port which is second port); and

Therefore, it would have been obvious to one of ordinary skilled in the art at the

time the invention was made to combine the teachings of Viswanath with the teachings

of Malakapalli in order to provide a system generating error detection and correction

information for data is provided in which at least one data sector is received and an

Input/Output Error Detection and Correction checksum (IOEDC), a Cyclic Redundancy

Code (CRC) and an ECC is generated from the at least one sector.

7.      Claims 2, 5, 10, 14 and 19, carry similar limitation as claim 1 above and

therefore, are rejected under for same rationale.

8.      As to claim 7, Viswanath and Malakapalli discloses the invention substantially as

applied to claims 1, 2 and 5 above, including, providing a portion of the electronic data

to a control module prior to deleting a portion of the electronic data (Viswanath, Fig.4,

Elements-84 and 64, Col.7, lines 17-21, where comparator 84 is control module, lines

32-33, where data is modified means deleting or adding header information and lines

37-39, where data is transferred to element-64, which is memory).

9.      As to claim 8, Viswanath and Malakapalli discloses the invention substantially as

in parent claim 7 above, including, wherein the portion of data provided to the control

module comprises the protocol header (Viswanath, Fig.1a and 1b, Col.3, lines 31-33,

Inherently protocol header is there, e.g. VLAN type, source address, destination

address etc.).

10.     As to claim 9, Viswanath and Malakapalli discloses the invention substantially as

applied to claims 1, 2, 5, 7 and 8 above, including, wherein the first port and the second

port comprise a receive port and a transmit port, respectively (Viswanath, Col.7, lines

10, where receiving port could be first port and lines 42-44, where output port is transmit

port).

11.     As to claim 11, Viswanath and Malakapalli discloses the invention substantially

as in parent claim 10 above, including, wherein the processor is further configured to

modify the electronic data prior to providing at least a portion of the electronic data to

one or more of the transmit ports (Viswanath, Col.7, lines 42-44, where out put port is

transmit port and VLAN insertion means the data has been modified).

12.     As to claim 12, Viswanath and Malakapalli discloses the invention substantially
as in parent claim 1 above, including, wherein the apparatus comprises a network
switch (Viswanath, Fig.2, Col.7, lines 10-11, where network switch means apparatus).

13.     As to claim 13, Viswanath Viswanath and Malakapalli discloses the invention
substantially as in parent claim 12 above, including, wherein said memory comprises
network switch internal memory (Viswanath, Fig.4, Element-64 and 80).

14.     As to claim 15, Viswanath and Malakapalli discloses the invention substantially
as in parent claim 11 above, including, wherein modifying the electronic data comprises
inserting a VLAN tag, wherein the VLAN tag relates at least in part to the destination
address of the electronic data (Viswanath, Col.7, lines 42-44, where VLAN tag is
inserted as a destination address).

15.     As to claim 16, Viswanath and Malakapalli discloses the invention substantially
as in parent claim 10 above, including, wherein the processor comprises a network
processor (Viswanath, Fig.3b, Element-70, Col.6, lines 25-26, where network switch has
decision making engine which is processor and since switch is a network device
therefore, processor is a network processor).

16.     As to claim 17, Viswanath and Malakapalli discloses the invention substantially
as in parent claim 10 above, including, wherein the memory comprises a plurality of
memory devices (Viswanath, Fig.3b, and Elements-32, 64 and 66, Col.5, lines 50-51
and 56).

17.　　As to claim 18, Viswanath and Malakapalli discloses the invention substantially

as in parent claim 17 above, including, wherein the plurality of memory devices

comprise one or more of:

　　　random access memory (Viswanath, Col.7, line 62) and

　　　synchronous dynamic random access memory (Viswanath, Col.5, lines 7-9).

18.　　Claims 23-26 are rejected for the same reasons as applied above to claims 5, 6

and 15-18 respectively.

19.　　As to claim 27, Viswanath and Malakapalli discloses the invention substantially

as in parent claim 19 above, including, wherein said processor is configured to modify

said electronic data only if said second port is configured to recognize tags (Viswanath,

Col.7, lines 10-13, where processor processes the tagged packets and lines 42-45,

transmitted to VLAN ports which means there are out put ports configured to handle

tagged packets).

20.　　As to claim 28, Viswanath and Malakapalli discloses disclose the invention

substantially as in parent claim 1 above, including, further comprising, the processor is

to generate a CRC of a non-discarded portion of the electronic data (Viswanath, Fig.4

Col.7, lines 10-29, where obviously destination tag is generated for the frame and not

for the striped tag).

21.　　Claims 29-30 has same limitations as of claim 28 and therefore, are rejected for

same rationale as applied to claim 28 above.

22.     As to claim 30-33, Viswanath and Malakapalli discloses the invention

substantially as in parent claims 1, 10 and 19, wherein the memory is internal to the

network device (Viswanath, Fig.2, element-34, where SDRAM is the internal memory).

23.     As to claims 34-36, memory is to comprise one or more queues and wherein

each of the one or more questions to be segmented into memory segments

corresponding to particular ports (Viswanath, Col.5, lines 50-57, Each of the MAC ports

60, 62 and 36 has a receive first-in-first-out (FIFO) buffer 64 and transmit FIFO buffer

66. Data packets from a network station are received by the corresponding MAC port

and stored in the corresponding receive FIFO buffer 64. The received data packet is

output from the corresponding receive FIFO buffer 64 to the external memory interface

32 for storage in the external memory 34, where FIFO buffer queues the packets which

has segmented to the corresponding MAC port.).

### *Conclusion*

**THIS ACTION IS MADE FINAL.**  Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action.  In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TAUQIR HUSSAIN whose telephone number is (571)270-1247. The examiner can normally be reached on 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thu Nguyen can be reached on 571 272 6967. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. H./
Examiner, Art Unit 2452


/THU NGUYEN/
Supervisory Patent Examiner, Art Unit 2452